Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **NOT O0**
3. **A1**
4. **NOT O1**
5. **A2**
6. **NOT O2**
7. **GND**
8. **NOT O5**
9. **A5**
10. **NOT O4**
11. **A4**
12. **NOT O3**
13. **A3**
14. **VCC**

**31 mils**

**2 1 14 13 12**

**3**

**4**

**5**

**11**

**10**

**9**

**6 7 8**

**AC04W**

**MASK**

**REF**

**25 mils**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential: GND (or leave FLOATING)**

**Mask Ref: AC04W**

**APPROVED BY: DK DIE SIZE .025” X .031” DATE: 12/4/17**

**MFG: FAIRCHILD SEMI THICKNESS .014” P/N: 54AC04**

**DG 10.1.2**

#### Rev B, 7/19/02